OIPE JC10
JAN 29 2004
PATENT & TRADEMARK OFFICE

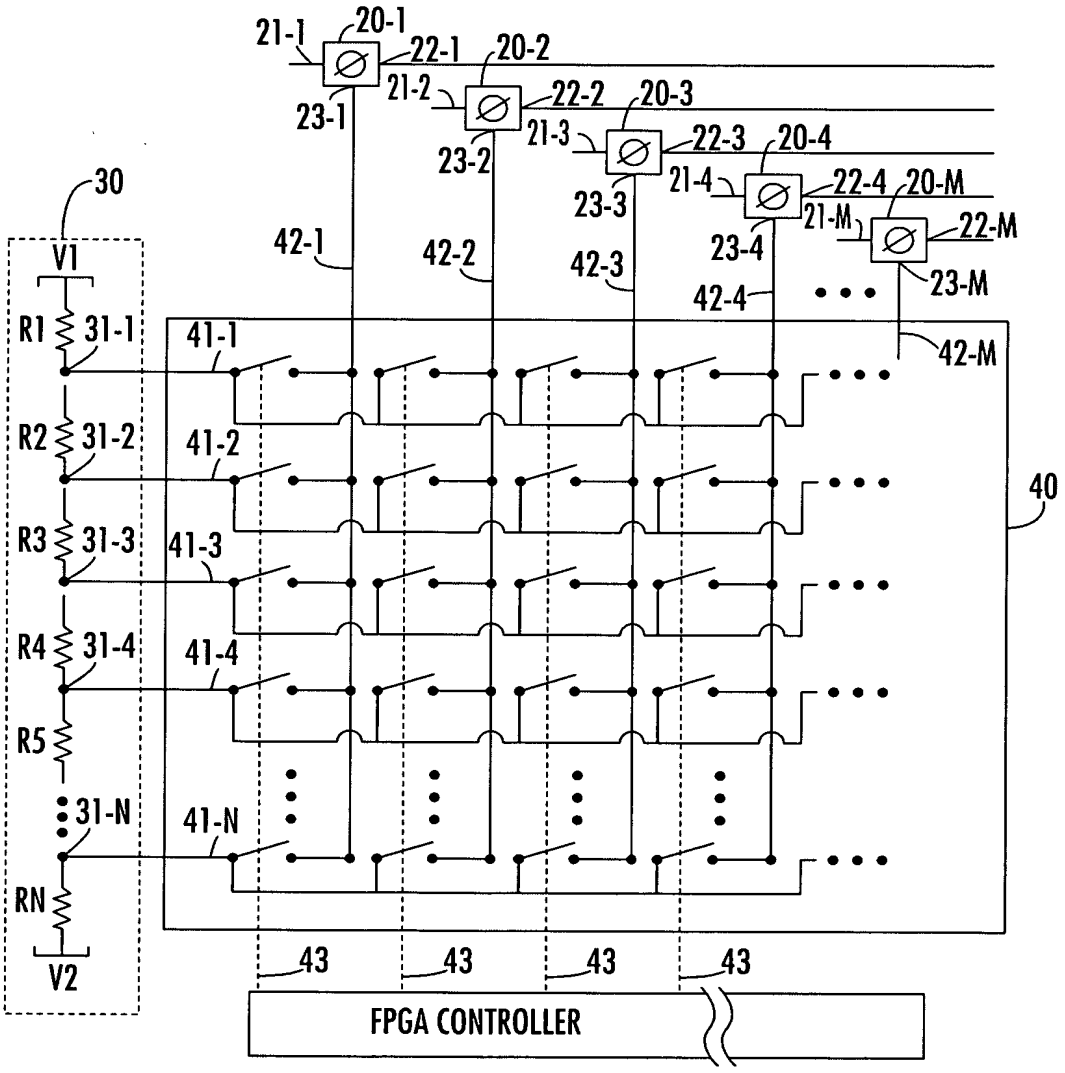
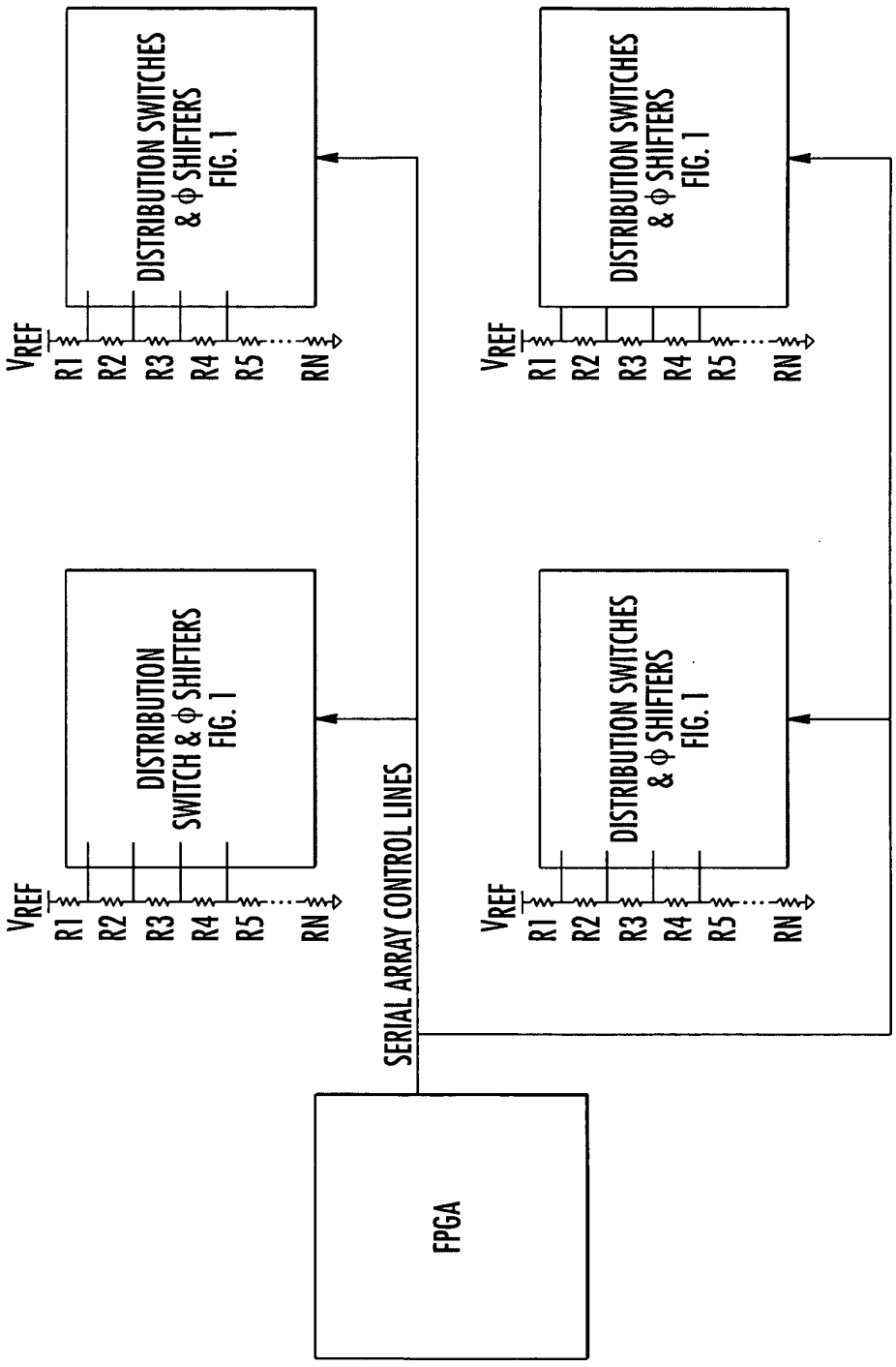


FIG. 1


DISTRIBUTION SWITCHES & φ SHIFTERS FIG. 1
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DISTRIBUTION SWITCH & φ SHIFTERS FIG. 1
DISTRIBUTION SWITCHES & φ SHIFTERS FIG. 1
VREF
R1
R2
R3
R4
R5
RN
SERIAL ARRAY CONTROL LINES
FPGA

FIG. 2